WHAT IS CLAIMED IS:

1. A memory comprising:

at least one array of memory elements;

a partition of the at least one array into a plurality of sub-arrays of the memory elements;

an array configuration circuit for selectively putting the at least one array in one of two operating configurations, the two operating configurations including:

a first operating configuration, in which the memory elements of the at least one array are coupled one to another to form a monodimensional sequentially-accessible memory, and

a second operating configuration, in which the memory elements in each sub-array are coupled to one another so as to form an independent monodimensional sequentially-accessible memory block, a data content of any memory element of the sub-array being rotatable by shifts through the memory elements of the sub-array;

a sub-array selector, responsive to a first memory address, for selecting one among the at least two sub-arrays according to the first memory address, the sub-array selector enabling access to the selected sub-array; and

a memory element access circuit, responsive to a second memory address, for enabling access to a prescribed memory element in the selected sub-array after a prescribed number of shifts, depending on the second memory address, of the data content of the memory elements in the selected sub-array.

2. The memory according to claim 1, in which said array configuration circuit includes, for each sub-array of memory elements, an input selector associated with a first memory element of the sub-array, for selectively feeding the first memory element with either an output of a last memory element in an adjacent previous sub-array, in the first operating configuration, or an output of a last memory element of the sub-array, in the second operating configuration.

3. The memory according to claim 1, in which the first operating configuration is a data storage configuration, in which the memory is put when data are to be stored therein, and the second operating configuration is a data retrieval configuration, in which the memory is put when data are to be retrieved therefrom.

4. The memory according to claim 3, in which in the second operating configuration each sub-array provides a respective output data, the sub-array selector selecting one sub-array output data out of the at least two output data provided by the at least two sub-arrays, according to the first address.

5. The memory according to claim 4, in which said memory element access circuit enables a transfer of the output data of the selected sub-array to a memory output after a prescribed number of shifts of the data content of the memory elements in the selected sub-array.

6. The memory according to claim 5, in which said memory element access circuit includes a counter for counting the number of data content shifts, and a coincidence detector detecting coincidence between a counter value and a value representative of the second address, the coincidence detector enabling the transfer of the output data of the selected sub-array to the memory output when the counter value equals the value representative of the second address.

7. The memory according to claim 1, in which each memory element includes at least one flip-flop.

8. A memory, comprising:

a plurality of memory locations each having a contents; and

a control circuit coupled to the memory locations and operable to,

allow random access to the memory locations during a first mode of operation, and

allow sequential access to the contents of the memory locations via a predetermined one of the memory locations during a second mode of operation.

9. The memory of claim 8 wherein:

the first mode of operation comprises a read mode; and

the second mode of operation comprises a write mode.

10. The memory of claim 8 wherein:

the first mode of operation comprises a write mode; and

the second mode of operation comprises a read mode.

11. A memory, comprising:

an array of memory locations; and

a control circuit coupled to the array and operable to cause the array to operate as

a random-access memory during a first mode of operation, and

a first-in-first-out memory during a second mode of operation.

12. The memory of claim 11 wherein:

the memory locations comprise a ring of serially coupled memory locations each having a respective contents; and

during the first mode of operation, the control circuit is operable to,

receive a clock signal,

shift the contents of each respective memory location in the ring to a respective next memory location in the ring once per cycle of the clock signal, and

allow access to a predetermined one of the memory locations during a predetermined cycle of the clock signal.

13. The memory of claim 11 wherein:

the memory locations comprise a ring of a number *n* of serially coupled memory locations each having a respective contents; and

during the first mode of operation, the control circuit is operable to,

receive a clock signal,

shift the contents of each respective memory location in the ring to a respective next memory location in the ring once per cycle of the clock signal for *n* clock cycles, and

allow access to a predetermined one of the memory locations during a predetermined cycle of the clock signal.

14. An electronic system, comprising:

a memory, comprising,

a plurality of memory locations each having a contents, and

a control circuit coupled to the memory locations and operable to,

allow random access to the memory locations during a first mode of operation, and

allow sequential access to the contents of the memory locations via a predetermined one of the memory locations during a second mode of operation.

15. A method, comprising:

randomly accessing memory locations of a memory during a first mode of operation, and

sequentially accessing the contents of the memory locations via a predetermined one of the memory locations during a second mode of operation.

16. The method of claim 15 wherein randomly accessing the memory locations comprises:

accessing a first memory location having a first address; and

accessing a second memory location having a second address.

17. The method of claim 15 wherein sequentially accessing the memory locations comprises:

reading first data from a first memory location;

shifting second data from a second memory location into the first memory location; and

reading the second data from the first memory location.

18. The method of claim 15 wherein sequentially accessing the memory locations comprises:

writing first data to a first memory location;

shifting the first data from the first memory location to a second memory location; and

writing second data to the first memory location.

19. The method of claim 15 wherein randomly accessing the memory locations comprises:

shifting the contents of each respective memory location to a respective next memory location a number of times; and

accessing a predetermined one of the memory locations after a predetermined one of the shifts.

20. The method of claim 15 wherein randomly accessing the memory locations comprises:

shifting the contents of each of *n* respective memory locations to a respective next one of the *n* memory locations *n* times; and

accessing a predetermined one of the *n* memory locations after a predetermined one of the *n* shifts.